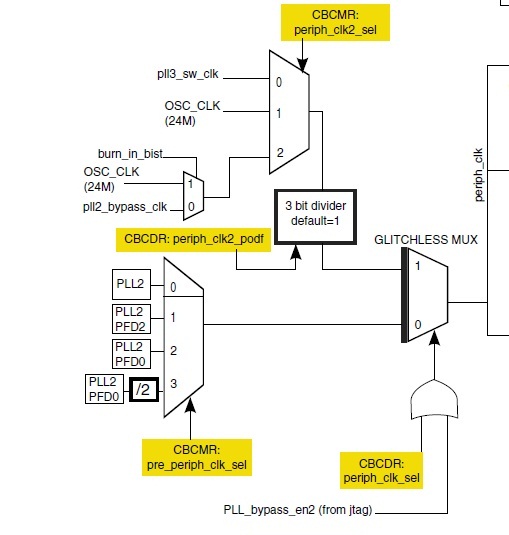
**Spread Spectrum**

**1. How to enable the feature**

Customer use imx6 Q/D/Solo for their projects, sometime they want to enable spread spectrum to pass EMI test on some frequency point. Imx6 support the spread spectrum feature, but only downward spread spectrum, for example if you want spread spectrum 9MHz on 400MHz frequency, the range will be 391MHz ~ 400MHz. Imx6 only has PLL2 support Spectrum spread, but PLL2 is the system PLL and several modules clocks come from it, the modules’ clock from PLL2 should not be impact by the frequency spread, customer should handle this part, need pay attention to the peripheral tolerance to frequency change. To enable the spread spectrum, the PLL2 need reconfigure, it need be shut down and enable/setting the spread spectrum and power on back again, during PLL2 offline period, we need another clock to replace PLL2 working temporary, then switch back to PLL2. We choice OSC\_CLK(24MHz) as the temporary system clock. Please see following PLL diagram.



Please see yellow part, those input values will decide where is the PLL clock come from, so from this diagram, we need set periph\_clik2\_sel to select OSC\_CLK, set periph\_clk\_set to switch to OSC\_CLK, before switch to OSC\_CLK, it need power down the PLL2 and set related settings for spread spectrum. After the settings, it need switch the clock from OSC\_CLK to PLL2 back. This setting procedure must be implemented before the DDR initialization, otherwise the system will hang due to change the DDR work clock.

There is file in uboot named flash\_headr.S which has the DDR initialization code which implement by DCD mode, under DCD mode, we can’t added the spread spectrum code, so we use another method called plugin, plugin will allow to execute code before the DDR initialization.

So here we added the code to enable the feature.

ldr r0, =CCM\_BASE\_ADDR

ldr r1, [r0,#0x18]

ldr r3, [r0,#0x18]

/\* set periph\_clik2\_sel to select OSC\_CLK \*/

and r1, r1, #0xffffcfff

orr r1, r1, #0x00001000

str r1, [r0,#0x18]

/\* set periph\_clk\_set to switch to OSC\_CLK \*/

ldr r1, [r0,#0x14]

ldr r2, [r0,#0x14]

orr r1, r1, #0x02000000

str r1, [r0,#0x14]

/\* power down PLL2 \*/

ldr r0, =0x020c8000

ldr r1, [r0,#0x30]

orr r1, r1, #0x00010000

str r1, [r0,#0x30]

/\* enable spread spectrum & configure \*/

ldr r1, =0x00001770

str r1, [r0,#0x60]

ldr r1, =0x05dc8006

str r1, [r0,#0x40]

ldr r1, [r0,#0x30]

and r1, r1, #0xFFFEFFFF

str r1, [r0,#0x30]

/\*need Delay short time before switch PLL2 it back\*/

ldr r4, =0x0

pu\_delay:

add r4, r4, #0x1

cmp r4, #0x200000

bne pu\_delay

/\* recovery the previous PLL source setting \*/

ldr r0, =CCM\_BASE\_ADDR

str r2, [r0,#0x14]

str r3, [r0,#0x18]

Above code enable the spread spectrum, then the next need change the DDR DCD code to assembly language code.

**2. How to config spread spectrum**

Spectrum spread will set two value according the following two formula, the modulation frequency is controlled about 48k, the range is controlled by user. We have verified 16MHz range can work.

Spectrum spread range = (ssc\_top)/DENOM \* Fref

Modulation frequency = Fref \* (ssc\_step)/(2\*ssc\_top)

e.g How to set 30Mspectrum spread

ldr r0, =0x020c8000

……

ldr r1, =0x00000960

str r1, [r0,#0x60]

ldr r1, =0x0bb88006

str r1, [r0,#0x40]

Fref is OSC clock 24MHz

0x00000960 is DENOM value

0bb8 is ssc\_top

0x8006, bit15 enable  spectrum spread， 0x6 is ssc\_step

**3. Merge code for rom code version**

The imx6 chipset has different rom code version, there is gap between different version, the gap will cause boot up issue when use plugin mode in uboot code. So please check your uboot code to see if you have the patch 0005-ENGR00285890-imx6-plugin-update-the-ROM\_API\_TABLE\_BA.patch.

**4. Weimnor offset**

Weimnor has different boot offset, need change this when use plugin mode. Please refer to example file flash\_header weimnor.S, please check the IVT change and return code

str r5, [r1]

mov r5, #0x1000 /\* Point to the second IVT table at offset 0x42C \*/

add r5, r5, #0x2C

str r5, [r2]

mov r0, #1

ivt\_header: .long 0x402000D1 /\*Tag=0xD1, Len=0x0020, Ver=0x40 \*/

app\_code\_jump\_v: .long 0x00908058 /\* Plugin entry point, address after the second IVT table \*/

reserv1: .long 0x0

dcd\_ptr: .long 0x0

boot\_data\_ptr: .long 0x00908020

self\_ptr: .long 0x00908000

app\_code\_csf: .long 0x0

reserv2: .long 0x0

boot\_data: .long 0x00907000

image\_len: .long 16\*1024 /\* plugin can be upto 16KB in size \*/

plugin: .long 0x1 /\* Enable plugin flag \*/